REMARKS

By the present amendment, claim 1 has been amended. Thus, after the present amendment, claims 1-7, 9-11, 13-21, and 32-34 remain in the present application. Reconsideration and allowance of outstanding claims 1-7, 9-11, 13-21, and 32-34 in view of the above amendments and following remarks are requested.

A. Rejection of Claims 1-7, 9-11, 13-21, and 32-34 under 35 USC §103(a)

The Examiner has rejected claims 1-7, 9-11, 13-21, and 32-34 under 35 USC §103(a) as being obvious with respect to U.S. Patent Number 5,922,065 to Hull, et al. ("Hull") and U.S. Patent Number 6,457,173 to Gupta, et al. ("Gupta"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claim 1, is patentably distinguishable over Hull and Gupta.

Various embodiments according to the present invention, as defined by amended independent claim 1, relate to decoding very long instruction word (VLIW) packets. Assembly code is provided for each one of a plurality of instructions in a first combination of instructions in a VLIW packet. A template is matched in the VLIW packet to a known template corresponding to one of a plurality of known syntaxes. The plurality of known syntaxes are arranged as a plurality of first level nodes in a tree structure. Each of a plurality of second level nodes in the tree structure includes a combination of instruction types. A plurality of paths extends between node levels, and each node of the plurality of first level nodes and the plurality of second level nodes has a

path to a node of a different node level. See. for example, Figure 2 of the present application.

Furthermore, each of a plurality of third level nodes in the tree structure includes an instruction type. One of the plurality of known syntaxes is matched with a resolved packet syntax using the tree structure. The resolved packet syntax is used to determine assembly code associated with execution of the first combination of instructions. Assembly code is then provided that is associated with execution of the first combination of instructions. Claim 1 has been amended to further illustrate aspects of the present invention. Specifically, claim 1 recites "wherein a plurality of paths extends between node levels and wherein each node of said plurality of first level nodes and said plurality of second level nodes has a path to a node of a different node level."

In contrast to the present invention as defined by amended independent claim 1, Hull discloses a processor that utilizes a template field for encoding a set of most useful instructions in a wide-word format. The instruction set of the processor comprises instructions that are one of a plurality of different instruction types. The execution units of the processor are also categorized into different types, wherein each instruction may be executed in one or more of the execution unit types. The instructions are grouped together into 128-bit sized and aligned containers referred to as bundles. Each bundle includes a plurality of instruction slots and a template field that specifies the mapping of the instruction slots to the execution unit types.

Nevertheless, as the Examiner states, correctly, Hull does not teach matching a template in a first composite packet to a known template corresponding to one of a plurality of known syntaxes, wherein the plurality of known syntaxes are arranged as a plurality of first level nodes in a tree structure, wherein each of a plurality of second level nodes in the tree structure includes a combination of instruction types, and wherein each of a plurality of third level nodes in the tree structure includes an instruction type. Hull also does not teach that the resolved packet syntax is determined using the known syntax.

Gupta does not cure the deficiencies of Hull. Gupta is directed to the automatic design of VLIW instruction formats. In Gupta, with the use of a computer the design of efficient binary instruction encodings of VLIW instruction formats is automated. The method involves automatically finding compact instruction formats that can express and exploit the full parallelism specified in the underlying processor microarchitecture.

Figure 2 of Gupta illustrates the structure of an if-tree. Column 12, lines 1-3 of Gupta simply state that the overall structure of the if-tree defines how each instruction is built. Figure 2 of Gupta illustrates "OR" nodes (oval-shaped) and "AND" nodes (boxed-shaped). Furthermore, Gupta states that "the OR nodes denote a selection between the children of the node such that only one choice (one branch) extends to the next level. Stated another way, each level of the tree is either a conjunction (AND) or disjunction (OR) of the subtrees at the lower level." Gupta, column 12, lines 7-13. Furthermore, in Figure 2 of Gupta, there are nodes that do not have paths to other node levels (i.e. there are dead ends).

This methodology in Gupta is not the same as that described with reference to Figure 2 of the present application. Contrast Gupta's methodology to amended independent claim 1, where a plurality of paths extends between node levels. Gupta actually teaches away from this methodology of a plurality of paths extending between node levels. Furthermore, in Figure 2 of the present application, all of the nodes have paths to other node levels (except for the level three nodes).

Gupta does not disclose, teach, or suggest the configuration of amended independent claim 1, including that a plurality of paths extends between node levels. Furthermore, there is no teaching or suggestion to combine of modify Gupta. Therefore, Gupta, singly or in combination with other art of record, does not disclose, teach, or suggest the present invention as defined by amended independent claim 1.

For the foregoing reasons, Applicant respectfully submits that the present invention as defined by amended independent claim 1 is not taught, disclosed, or suggested by the art of record. Thus, amended independent claim 1 is patentably distinguishable over the art of record. As such, the claims depending from amended independent claim 1 are, *a fortiori*, also patentable for at least the reasons presented above and also for additional limitations contained in each dependent claim.

B. Conclusion

Based on the foregoing reasons, the present invention, as defined by amended independent claim 1, and the claims depending therefrom, is patentably distinguishable

over the art cited by the Examiner. Thus, outstanding claims 1-7, 9-11, 13-21, and 32-34 are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance Notice of Allowance directed to all claims 1-7, 9-11, 13-21, and 32-34 remaining in the present application is respectfully requested.

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Respectfully Submitted,
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